Kai-hui Chang

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Objective

A faculty, research or engineering position where ten years of successful experience in logic simulation, functional verification and physical synthesis will be of value.

Professional Skills

Programming Languages: Verilog, C, C++, Pascal, Java, Perl, Shell Scripts.
Platforms: Linux, Windows.
EDA Software: Synopsys Design Compiler, Synopsys TetraMax, Verilog simulators.

Education

University of Michigan, Ann Arbor, MI 2004 to 2007
Ph. D., Computer Science and Engineering. GPA: 8.3/9.0.
Advisors: Prof. Igor Markov and Prof. Valeria Bertacco

National Taiwan University, Taipei, Taiwan 1999 to 2001
M. S., Electrical Engineering. GPA: 4.0/4.0. Rank: 5/142. Advisor: Prof. Sy-yen Kuo

National Taiwan University, Taipei, Taiwan 1995 to 1999
B. S., Electrical Engineering. GPA: 3.9/4.0. Rank: 3/159.

Work Experience

Senior Technical Staff 2008 to present
Avery Design Systems, Andover, MA, USA

- Enhanced Insight, an RTL symbolic simulator, to support SystemVerilog assertion and coverage features.
- Integrated Boolean solvers into Insight and improved its performance by 100-1000X.
- Developed innovative solutions for X-verification, reset slack analysis, reset reduction, FSM analysis and design for testability problems.
- Advised three Ph. D. students in Taiwan, graduated one of them, and published more than 10 peer-reviewed technical papers.
- Provided specialized solutions for customer problems and supported evaluations.
- Successfully promoted Avery's tools for customers in Japan.

Project Manager 2003 to 2004
Avery Design Systems, Taipei, Taiwan. (Headquartered in Andover, MA, US.)

- Managed SimCluster (a parallel simulator) development team with the US headquarter.
- Worked with customers in the US and accelerated their simulation by 2-13X.

Software Engineer 2001 to 2003
Avery Design Systems, Taipei, Taiwan. (Headquartered in Andover, MA, US.)

- Developed a simulation-based temporal assertion checker which runs up to 10X faster than competing checkers.
- Improved the speed of SimCluster by more than 200%.
- Codeveloped one of the first PCI-X/PCI-Express verification IPs in market, which has been used by more than 20 design houses.

Research Experience

Ph. D. Thesis: Functional Design Error Diagnosis, Correction and Layout Repair of Digital Circuits

- Automatically reduces the complexity of bug traces for easier bug analysis.
- Automatically repairs functional errors in RTL/gate-level designs and implements error corrections in layouts.
- Comprehensively generates various layout transformations to repair electrical errors.
- InVerS: a flexible and efficient combinational/sequential verification methodology.

M.S. Thesis: A Compiled-Code Technique for RTL Designs

- Developed a compiled-code RTL Verilog simulator based on an interpreted version.

Kai-hui Chang

Honors

ACM SIGDA Outstanding Dissertation Award at DAC, 2009.

EDAA Outstanding Dissertation Award at DATE, 2008.

Second Place – ICCAD Cadathlon, 2006.

First Place – IEEE IWLS Programming Challenge, 2006.

Patents

K.-H. Chang, Y.-T. Liu, C. Browy and C. Huang, "System and Method for Correcting Gate-level Simulation When Unknowns Exist", United States Patent Application 13477743, May 22, 2012

K.-H. Chang, I. Wagner, V. Bertacco, and I. L. Markov, "Automatic Error Diagnosis and Correction for RTL Designs", States Patent Application 20080295043, Nov. 27, 2008

Book

K.-H. Chang, I. L. Markov, V. Bertacco, "Functional Design Errors in Digital Circuits: Diagnosis, Correction and Repair", Springer 2009. (ISBN: 978-1-4020-9364-7)

Affiliations

Association for Computing Machinery (ACM).

Institute of Electrical and Electronics Engineers (IEEE).

Professional Service

Ph. D. committees: *Hong-zu Chou, National Taiwan University, Jun. 2010*

Technical committee members: *ACM/IEEE Intl. Workshop on Logic and Synthesis (IWLS),* since 2011; *ACM/IEEE Intl. Conf. on Computer-Aided Design of Integrated Circuits (ICCAD)*, 2011

Reviewer for journals: *IEEE Trans. on CAD, ACM Trans. on Design Automation, IEEE Trans. on VLSI, IEEE Transactions on Circuits and Systems II*

Reviewer for conferences: *ACM/IEEE Intl. Conf. on Computer-Aided Design (ICCAD), IEEE/ACM Design Automation & Test in Europe (DATE),ACM/IEEE Asia and South Pacific Design Automation Conference (ASPDAC), ACM/IEEE Design Automation Conf. (DAC)*

Selected Publications

(The complete list of publications is available at http://www.kaihuichang.com/)

Functional Verification and Automatic Debugging

1. **K.-H. Chang**, H.-Z. Chou, H. Yu, D. Dobbyn and S.-Y. Kuo, "Handling Nondeterminism in Logic Simulation So That Your Waveform Can Be Trusted Again", *IEEE Design and Test of Computers*, to appear
2. **K.-H. Chang**, C.-W. Chang, J.-H. R. Jiang and C.-N. J. Liu, "Improving Design Verifiability by Early RTL Coverability Analysis", *ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, Arlington, VA, Jul. 2012, to appear
3. **K.-H. Chang** and C. Browy, "Improving Gate-level Simulation Accuracy when Unknowns Exist", *Design Automation Conference (DAC)*, San Francisco, CA, Jun. 2012, pp. 936-940
4. C.-W. Chang, H.-Z. Chou, **K.-H. Chang**, J.-H. R. Jiang, C.-N. J. Liu, C.-H. Hsiao and S.-Y. Kuo, "Constraint Generation for Software-Based Post-Silicon Bug Masking with Scalable Resynthesis Technique for Constraint Optimization", *Proc. Int'l Symposium on Quality Electronic Design (ISQED)*, Santa Clara, CA, Mar 2011, pp. 174-181
5. H.-Z. Chou, **K.-H. Chang** and S.-Y. Kuo, "Facilitating Unreachable Code Diagnosis and Debugging", *Proc. Asia and South Pacific Design Automation Conf. (ASPDAC)*, Yokohama, Japan, January 2011, pp. 485-490
6. H.-Z. Chou, H. Yu, **K.-H. Chang**, D. Dobbyn and S.-Y. Kuo, "Finding Reset Nondeterminism in RTL Designs – Scalable X-Analysis Methodology and Case Study", *Proc. Design Autom. and Test in Europe (DATE)*, Dresden, Germany, Mar. 2010, pp. 1494-1499
7. **K.-H. Chang**, D. A. Papa, I. L. Markov, V. Bertacco, "InVerS: An Incremental Verification System with Circuit Similarity Metrics and Error Visualization", *IEEE Design and Test of Computers*, Mar, 2009, pp. 34-43

8. H.-Z. Chou, I.-H. Lin, C.-S. Yang, **K.-H. Chang** and S.-Y. Kuo, "Enhancing Bug Hunting Using High-Level Symbolic Simulation", *Great Lakes Symp. on VLSI (GLSVLSI)*, Boston, MA, May 2009, pp. 417-420
9. **K.-H. Chang**, I. L. Markov and V. Bertacco, "Automating Post-Silicon Debugging and Repair", *IEEE Computer*, vol. 41, no. 7, Jul. 2008, pp. 47-54
10. **K.-H. Chang**, I. L. Markov and V. Bertacco, "Fixing Design Errors with Counterexamples and Resynthesis", *IEEE Trans. on Computer-Aided Design (TCAD)*, Jan. 2008, pp. 184-188
11. **K.-H. Chang**, I. L. Markov, and V. Bertacco, "Automating Post-Silicon Debugging and Repair", *Proc. Int'l Conf. Computer-Aided Design (ICCAD)*, Nov. 2007, pp. 91-98
12. **K.-H. Chang**, I. Wagner, V. Bertacco, and I. L. Markov, "Automatic Error Diagnosis and Correction for RTL Designs", *Proc. IEEE Int'l High Level Design Validation and Test Workshop (HLDVT)*, Nov. 2007, pp. 65-72
13. **K.-H. Chang**, D. A. Papa, I. L. Markov and V. Bertacco, "InVerS: An Incremental Verification System with Circuit Similarity Metrics and Error Visualization", *Proc. Int'l Symp. on Quality Electronic Design (ISQED)*, Mar. 2007, pp. 487-492
14. **K.-H. Chang**, V. Bertacco and I. L. Markov, "Simulation-based Bug Trace Minimization with BMC-based Refinement", *IEEE Trans. on Computer-Aided Design (TCAD)*,Vol. 26, NO. 1, Jan. 2007, pp. 152-165
15. **K.-H. Chang**, V. Bertacco and I. L. Markov, "Simulation-based Bug Trace Minimization with BMC-based Refinement", *Proc. Int'l Conf. Computer-Aided Design (ICCAD)*, 2005, pp. 1045-1051
16. **K.-H. Chang**, W.-T. Tu, Y.-J. Yeh, and S.-Y. Kuo, "A Temporal Assertion Extension to Verilog," *Proc. International Symposium on Automated Technology for Verification and Analysis (ATVA04)*, Oct. 2004, Taipei, Taiwan, LNCS 3299, pp 499-504

Logic Synthesis and Design Optimization

17. C.-N. Chung, C.-W. Chang, **K.-H. Chang** and S.-Y. Kuo, "Applying Verification Intention for Design Customization via Property Mining under Constrained Testbenches", Proc. *ACM/IEEE Intl. Conf. Computer Design (ICCD)*, Amherst, MA, 2011, pp. 84-89.
18. C.-N. Chung, C.-W. Chang, **K.-H. Chang** and S.-Y. Kuo, "Formal Reset Recovery Slack Calculation at the Register Transfer Level", *Proc. Design Autom. and Test in Europe (DATE)*, Grenoble, France, Mar. 2011, pp.571-574
19. **K.-H. Chang**, V. Bertacco, I. L. Markov and A. Mishchenko, "Logic Synthesis and Circuit Customization Using Extensive External Don't-Cares", *ACM Trans. on Design Automation of Electronic Systems (TODAES)*, Vol. 15, No. 3, Article 26, 2010
20. H.-Z. Chou, **K.-H. Chang** and S.-Y. Kuo, "Accurately Handle Don't-Care Conditions in High-Level Designs and Application for Reducing Initialized Registers", *IEEE Trans. on Computer-Aided Design (TCAD)*, Apr. 2010, pp. 646-651
21. H.-Z. Chou, **K.-H. Chang** and S.-Y. Kuo, "Optimizing Blocks in an SoC Using Symbolic Code-Statement Reachability Analysis", *Proc. Asia and South Pacific Design Automation Conf. (ASPDAC)*, Taipei, Taiwan, January 2010, pp. 787-792
22. H.-Z. Chou, **K.-H. Chang** and S.-Y. Kuo, "Handling Don't-Care Conditions in High-Level Synthesis and Application for Reducing Initialized Registers", *Design Automation Conference (DAC)*, San Francisco, CA, July 2009, pp. 412-415
23. **K.-H. Chang**, V. Bertacco, I. L. Markov, "Customizing IP Cores for System-on-Chip Designs Using Extensive External Don't-Cares", *Proc. Design Autom. and Test in Europe (DATE)*, Nice, France, April 2009, pp. 582-585
24. **K.-H. Chang**, I. L. Markov, and V. Bertacco, "Reap What You Sow: Spare Cells for Post-Silicon Metal Fix", *Proc. Int'l Symposium on Physical Design (ISPD)*, Portland, OR, Mar. 2008, pp. 103-110
25. **K.-H. Chang**, I. L. Markov, V. Bertacco, "SafeResynth: A New Technique for Physical Synthesis", *Integration: the VLSI Journal*, Jul. 2008, pp. 544-556

26. **K.-H. Chang**, I. L. Markov and V. Bertacco, "Post-Placement Rewiring by Exhaustive Search For Functional Symmetries", *ACM Trans. on Design Automation of Electronic Systems (TODAES)*, Vol. 12, No. 3, Article 32, Aug. 2007
27. **K.-H. Chang**, I. L. Markov and V. Bertacco, "Safe Delay Optimization for Physical Synthesis", *Proc. Asia and South Pacific Design Automation Conf. (ASPDAC),* Yokohama, Japan, Jan. 2007, pp. 628-633
28. **K.-H. Chang**, I. L. Markov and V. Bertacco, "Post-Placement Rewiring and Rebuffering by Exhaustive Search For Functional Symmetries',' *Proc. Int'l Conf. Computer-Aided Design (ICCAD)*, Nov. 2005, pp. 56-63

Parallel Simulation

29. **K.-H. Chang** and C. Browy, "Parallel Logic Simulation -- A Myth or Reality?", *IEEE Computer*, vol. 45, no. 4, Apr. 2012, pp. 67-73
30. **K.-H. Chang** *et al.*, "Automatic Partitioner for Behavior Level Distributed Logic Simulation", *Proc. Int'l Conf. Formal Techniques for Networked and Distributed Systems (FORTE)*, Oct. 2005, Taipei, Taiwan, LNCS 3731, pp 525-528
31. **K.-H. Chang** *et al.*, "Techniques to Reduce Synchronization in Distributed Parallel Logic Simulation", *Proc. IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS'04)*, Cambridge, MA, Nov. 2004

Testing

32. **K.-H. Chang**, C.-W. Chang, J.-H. R. Jiang and C.-N. J. Liu, "Reducing Test Point Overhead Using Don't-Cares", *IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, Boise, ID, Aug. 2012, to appear
33. **K.-H. Chang**, H.-Z. Chou and I. L. Markov, "RTL Analysis and Modifications for Improving At-speed Test", *Proc. Design Autom. and Test in Europe (DATE)*, Dresden, Germany, March 2012, pp. 400-405